REMARKS/ARGUMENTS

Claims 24-26, 29-35 and 38-43 remain in this application. Claims 1-23, 27-28 and 36-37 have been cancelled without prejudice. Claims 24, 33 and 38 are amended to make the claimed inventions more specific.

The Examiner is thanked for the thorough examination of the present application. Applicants have made an amendment to the claims, and assert that the remaining claims are patentable for at least the reasons set forth herein.

Response to the drawing objection:

Applicant respectfully asserts that the drawings of the specification of the present application have shown every feature of the invention specified in the claims. As for claim 24, it recites:

> "[A]n apparatus (*figs. 1, 2A, 2C and 6 for the first embodiment; figs. 3, 4, and 6 for the second embodiment*) for automatically determining a type of an external device, comprising: a jack (*15; 41*) for coupling the external device;
>
> an impedance detecting circuit (*13; 401*), coupled to the external device through the jack (*15; 41*), for generating a first analog signal (*DCVOL when transistor Q1 being turned on as shown in fig. 2A, hereafter "DCVOL1"; DC-Sense when connecting switch SW1 with resistor R3 as shown in fig. 4, hereafter "DC-Sense1"*) according to an impedance of the external device and a first resistance (*R3 of figs. 2A and 4*), a second analog signal (*DCVOL when transistor Q2 being turned on, hereafter "DCVOL2" as shown in fig. 2A; DC-Sense when connecting switch SW1 with resistor R4 as shown in fig. 4, hereafter "DC-Sense2"*) according to the impedance of the external device and a second resistance (*R4 of figs. 2A and 4*) and a third analog signal

(*DCVOL when transistor Q3 being turned on as shown in fig. 2A, hereafter "DCVOL3"; DC-Sense when connecting switch SW1 with resistor R5 as shown in fig. 4, hereafter "DC-Sense3"*) according to the impedance of the external device and a third resistance (*R5 of figs. 2A and 4*), wherein the first, second and third resistances (*R3, R4, R5*) are different;

an analog-to-digital converter (*14; 404*), coupled to the impedance detecting circuit (*13; 401*), for converting the first, second and third analog signals (*DCVOL1, DCVOL2, DCVOL3; DC-Sense1, DC-Sense2, DC-Sense3*) to first, second and third digital values (*referring to the second paragraph of page 9 and fig. 6 which recites that "...the first voltage dividing value also corresponds to 13-15 when the voltage value is converted to a 4-bit digital number..."*), respectively; and

a control circuit (*11; 402*), coupled to the analog-to-digital converter (*14; 404*), for determining the type of the external device when the first digital value falls within a first predetermined range (*col. DCVOL1 in Fig. 6*), the second digital value falls within a second predetermined range (*col. DCVOL2 in Fig. 6*), the third digital value falls within a third predetermined range (*col. DCVOL3 in Fig. 6*) and all of the first, second and third predetermined ranges together indicate a same recognized condition (*col. Recognized Condition in Fig. 6*) among a plurality of predetermined recognized conditions (*col. Recognized Condition in view of rows Power Speaker1, Power Speaker2, Earphone, Microphone, CD-ROM and Player in Fig. 6*);

wherein the impedance detecting circuit (*13; 401*) comprises a plurality of resistors (*R3, R4, R5*), which couples together in parallel, for providing the first, second and third resistance (*R3, R4, R5*).

(*descriptions and element labels added*)

Accordingly, every feature of claim 24 has been shown in the drawings. Similarly, the features of the other claims have been depicted in the drawings. Therefore, a withdrawal of the drawing objection is respectfully requested.

Response to the 35 U.S.C. § 112 rejections:

Please refer to the third paragraph of page 5 of the original specification which recites that "[T]he output signal of the controlling device 11 can first feed into a decoding device 12, and then couple to the detecting device 13 and the multiplexer 16, in order to reduce the number of outputs of the controlling device 11. As shown in Fig. 2B, the decoding device 12 can be a 3 to 8 decoder (3x8 decoder)". Accordingly, claim 43 is supported by the original specification. Therefore, a withdrawal of the 35 U.S.C. § 112 rejections is respectfully requested.

Response to the 35 U.S.C. § 102(e) rejections:

Claims 24-26, 29-33 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Patterson et al. (U.S. Patent Appl. Pub. No. 2004/0081099, hereafter "Patterson"). Applicant has carefully read Patterson and found that Patterson discloses **a plurality of jacks** (60a' to 60n' in fig. 17) **respectively** connecting to **one** of the resistors (R1 to RN in fig. 17) of a resistive ladder (410b in fig. 17). However, Patterson nowhere teaches or suggests how to generate a first analog signal according to a first resistor (such as R1) and an impedance of an external device coupled to the resistive ladder (410b) through a jack (such as 60a'), generate a second analog signal according to a second resistor (such as R2) and the impedance of **the same external device** coupled to the resistive ladder (410b) through **the same jack (60a')**, and generate a third analog signal according to a third resistor (such as R3) and the impedance of **the same external device** coupled to the

resistive ladder (410b) through **the same jack (60a')**. Please note that the assumed first, second and third analog signals of Patterson must be generated according to the impedance of **the same external device** coupled to the resistive ladder (410b) through **the same jack** (60a') so as to accord with the claimed impedance detecting circuit. Accordingly, Patterson fails to disclose the claimed impedance detecting circuit in structure and function and consequently fails to disclose the claimed invention.

Furthermore, Patterson also fails to teach or suggest the claimed features as follows: "a control circuit for determining the type of an external device when a first digital value converted from the first analog signal falls within a first predetermined range, a second digital value converted from the second analog signal falls within a second predetermined range, the third digital value converted from the third analog signal falls within a third predetermined range and **all of the first, second and third predetermined ranges together indicate a same recognized condition among a plurality of predetermined recognized conditions, wherein each of the first, second and third digital values is a multi-bit number**". Patterson at most describes that "[I]nside codec 11, low resolution analog to digital converter (ADC) 412 measures **the voltage on JS pin node** 400. When the voltage level changes, a device was plugged into or removed from a jack 60 in the system connected to the resistor ladder network 410. ADC 412 **sends the voltage measurement to software that determines what jack the event happened** and if something was plugged in or out, based on the voltage level at JS pin node 400 (Patterson: Page 7[0071])." and "[T]he identification process can be understood more readily with reference to the jack sensing table in FIG. 10 where it can be seen that such devices as speakers, headphones, mono headsets, SPDIF or digital speakers, telecommunications devices or a microphone respectively, are **represented by a distinctive three-bit digital code as listed in the columns JS1, JS3, and JS0** (Patterson: Page 6[0060])." But Patterson neither teaches that each of the JS1, JS3 and JS0 (a single-bit digit) is a multi-bit number so as to fall within **a predetermined RANGE** instead of just a logic high-low difference, nor discloses that **the predetermined RANGES**, which are **not the**

JS1, JS3 and JS0 themselves but the ranges they fall within, together indicate a same recognized condition among a plurality of predetermined recognized conditions. Therefore, Patterson does not disclose the claimed control circuit.

For at least the reasons mentioned above, applicant respectfully asserts that claims 24-26, 29-33 and 35 are patentable over Patterson.

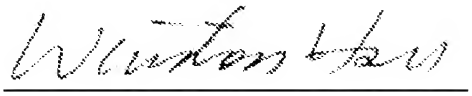
Response to the 35 U.S.C. § 103(a) rejections:

Claims 34 and 38-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patterson in view of Dao (U.S. Pat. No. 6,407,633). Applicant respectfully asserts that Patterson fails to teach or suggest "a control circuit for determining the type of an external device when a first digital value converted from the first analog signal falls within a first predetermined range, a second digital value converted from the second analog signal falls within a second predetermined range, the third digital value converted from the third analog signal falls within a third predetermined range and **all of the first, second and third predetermined ranges together indicate a same recognized condition among a plurality of predetermined recognized conditions, wherein each of the first, second and third digital values is a multi-bit number**" because of the same explanation described before, and Dao fails to compensate for the deficiency of Patterson. Therefore, claims 34 and 38-43 are patentable over Patterson in view of Dao.

Conclusion:

Therefore, all pending claims are submitted to be in condition of allowance. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

Sincerely yours,



Date: 07/11/2008

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